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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,509	07/16/2003	Minoru Maeda	14815-015001	8467

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,509	MAEDA, MINORU	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-5 are presented in the instant application according to the Applicant's filing on 07/16/2003.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings Objection

2. The drawings are objected to because of lacking "Prior Art" label in figure 5. Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Abstract

3. The amended abstract of the disclosure is objected to because it contains two separate paragraphs. Correction is required. See MPEP § 608.01(b).

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "**means**" and "**said**," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

Claim Objections/Minor Informalities

5. Claims 3-5 are objected to because of the following informalities:

Claim 3:

Line 9, there is no express antecedent basis for "said second voltage controlled oscillator". It is suggested that "said" be changed to -- a --;

Line 7, delete DDS and insert --direct digital synthesizer (DDS) --.

Claim 4:

Line 10, there is no express antecedent basis for "said second voltage controlled oscillator". It is suggested that "said" be changed to -- a --;

Line 7, delete DDS and insert --direct digital synthesizer (DDS) --.

Claim 5:

Line 3, there is no express antecedent basis for "the front stage". It is suggested that "said" be changed to -- a --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1 and 2, line 8 and line 9, respectively, the recitation "...PLL stage ..., through a low-pass filter", renders the claim indefinite since the drawings illustrate a band-pass filter and *not* a low-pass filter.

Clarification is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heymann (U.S. Patent No. 6,611,675) in view of Jackson et al. (U.S. Patent No. 6,366,620).

With respect to claims 1 and 5, as best understood, Heymann discloses, in Fig. 1, a phase locked loop circuit using a fractional frequency divider comprising a) a first PLL stage [First Phase Locked Loop] for controlling the output frequency of a first voltage-controlled oscillator [7] with a deviation, which is obtained by dividing the frequency of the output of the first voltage-controlled oscillator by a first fractional frequency divider [Main Divider (8) which encompasses fractional divider] and by comparing [5] the frequency-divided output with a reference frequency; and b) a second fractional frequency divider [Reference Divider (9) which encompasses fractional divider] for dividing the f frequency of the output of the first PLL stage and for inputting the frequency-divided output as a reference frequency signal of a second PLL stage [Second Phase Locked Loop], in which the output signal of a second voltage-controlled oscillator [14] of the second PLL stage is extracted.

Heymann fails to disclose comparing the frequency-divided output with a reference frequency, through a band-pass filter *(as shown in drawings)*.

Jackson et al. discloses, in Fig. 3, a phase locked loop with a phase detector for comparing a frequency-divided output with a reference frequency, through a band-pass filter [38].

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure Heymann's phase locked loop having a phase locked loop with a phase detector for comparing a frequency-divided output with a reference frequency, through a band-pass filter to further filter the divided output signal since such circuit arrangement of the phase locked loop circuit for the stated purpose has been a well known practice as evidenced by the teachings of Jackson et al.

With respect to claims 2 and 5, as best understood, Heymann discloses, in Fig. 1, that the second PLL stage is constructed to control the output frequency of the second voltage-controlled oscillator [14] with a deviation, which is obtained by dividing the frequency of the output of the second voltage-controlled oscillator by frequency divider [Main Divider (12) and divider (13), which encompasses fractional divider] and by comparing the frequency-divided output with the reference frequency, through a band-pass filter *(as shown in drawings)*.

Heymann fails to disclose comparing the frequency-divided output with a reference frequency, through a band-pass filter *(as shown in drawings)*.

Jackson et al. discloses, in Fig. 3, a phase locked loop with a phase detector for comparing a frequency-divided output with a reference frequency, through a band-pass filter [38].

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure Heymann's phase locked loop having a phase locked loop with a phase detector for comparing a frequency-divided output with a reference frequency, through a band-pass filter to further filter the divided output signal since such circuit arrangement of the phase locked loop circuit for the stated purpose has been a well known practice as evidenced by the teachings of Jackson et al.

10. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heymann (U.S. Patent No. 6,611,675) in view of Takao (JP Patent No. 06-209216).

With respect to claim 3, Heymann discloses, in Fig. 1, a phase locked loop circuit using a fractional frequency divider [dividers 8,12, and 13, encompassing fractional divider] comprising a) a first PLL stage [First Phase Locked Loop] for controlling the output frequency of a first voltage-controlled oscillator [7] in accordance with a deviation, which is obtained by comparing the output of the first voltage-controlled oscillator with a reference frequency and b) a second PLL stage [Second Phase Locked Loop] for controlling the output frequency of the second voltage-controlled oscillator [14] in accordance with a deviation, which is obtained by using the output of the first PLL stage as a reference frequency signal and by comparing [10] the output of a second voltage-controlled oscillator divided in frequency by a fractional frequency divider [dividers 12 and 13, encompassing fractional divider], with the reference frequency signal, wherein the output signal of a second voltage-controlled oscillator of the second PLL stage extracted.

Heymann fails to disclose comparing the output of the first voltage-controlled oscillator with a reference frequency through a DDS (Direct Digital Synthesizer). Instead, Heymann discloses comparing the output of the first voltage-controlled oscillator with a reference frequency through a frequency divider.

Takao discloses, in Fig. 1, a phase locked loop including a DDS, having a frequency-divider function *(see Abstract line 7-8),* for providing a frequency divided output to be compared with a reference frequency signal by phase detector [2].

To configure Heymann's phase locked loop with a DDS having frequency-divider function in lieu of a frequency divider as taught by Takao to obtain the desired frequency resolution would have been obvious to one of ordinary skill in the art at the time of the invention since Takao teaches that by utilizing such DDS circuit would provide higher frequency resolution thus provides better synchronization *(see Takao, page 3 of translation).*

With respect to claim 4, Heymann discloses, in Fig. 1, a phase locked loop circuit using a fractional frequency divider comprising a) a first PLL stage [First Phase Locked Loop] for controlling the output frequency of a first voltage-controlled oscillator [7] with a deviation, which is obtained by dividing the frequency of the output of the first voltage-controlled oscillator by a first fractional frequency divider [8, which encompasses fractional divider] and by comparing the frequency-divided output with a reference frequency; and b) a second PLL stage [Second Phase Locked Loop] for controlling the output frequency of the second voltage-controlled oscillator in accordance with a deviation, which is obtained by using the output of the first PLL stage as a reference frequency signal and by comparing the output of a second voltage-

controlled oscillator with the reference frequency signal, wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.

Heymann fails to disclose comparing the output of the second voltage-controlled oscillator with a reference frequency through a DDS (Direct Digital Synthesizer). Instead, Heymann discloses comparing the output of the first voltage-controlled oscillator with a reference frequency through a frequency divider.

Takao discloses, in Fig. 1, a phase locked loop including a DDS, having a frequency-divider function *(see Abstract line 7-8),* for providing a frequency divided output to be compared with a reference frequency signal by phase detector [2].

To configure Heymann's phase locked loop with a DDS having frequency-divider function in lieu of a frequency divider as taught by Takao to obtain the desired frequency resolution would have been obvious to one of ordinary skill in the art at the time of the invention since Takao teaches that by utilizing such DDS circuit would provide higher frequency resolution thus provides better synchronization *(see Takao, page 3 of translation).*

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heymann (U.S. Patent No. 6,611,675) in view of Takao (JP Patent No. 06-209216) as applied to claims 1-4 above, and further in view of Jackson et al. (U.S. Patent No. 6,366,620).

With respect to claim 5, the combination of Heymann and Takao discloses all of the claimed limitations as expressly recited in claims 3 and 4 *(for dependency on claims 1-2, see 103(a) rejection of claims 1 and 2)*, except for a band-pass filter inserted into a front stage of a phase comparator of the first PLL stage.

Jackson et al. discloses, in Fig. 3, a phase locked loop with a phase detector for comparing a frequency-divided output with a reference frequency, through a band-pass filter [38].

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a phase locked loop having a phase locked loop with a phase detector for comparing a frequency-divided output with a reference frequency, as disclosed via the combined teachings of Heymann and Takao, through a band-pass filter to further filter the divided output signal since such circuit arrangement of the phase locked loop circuit for the stated purpose has been a well known practice as evidenced by the teachings of Jackson et al.

Citation of Relevant Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Hirata et al. (U.S. Patent No. 5,353,311) discloses a radio transmitter including two phase locked loops connected in series.

Prior art Troxel (U.S. Patent No. 4,806,879) discloses a method and apparatus for synchronizing to a pulse train packet signal.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN